UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,396	01/18/2002	Santosh C. Lolayekar	E003-1005US0	8983

48789 7590 05/02/2007

LAW OFFICES OF BARRY N. YOUNG
260 SHERIDAN AVENUE
SUITE 410
PALO ALTO, CA 94306-2047

EXAMINER	
GREY, CHRISTOPHER P	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
05/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/051,396	LOLAYEKAR ET AL.	
	Examiner	Art Unit	
	Christopher P. Grey	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-23* is/are allowed.

6)☒ Claim(s) *1-18 and 24-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The applicant claims that step a and b occur without buffering the packet **within the switch**. The examiner does not see where within the specification no buffering is performed within the switch. The examiner points to page 18 para 0078, where no buffering is performed within the PPU, where the PPU is a component within the switch. Furthermore, page 20 para 0085 clearly indicated buffering within the switch (a large buffer to queue cells for delivery).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as it recites the limitation "all of the steps" in line 1. There is insufficient antecedent basis for this

limitation in the claim. The claim makes reference to all of the steps, however, the preceding claims do not specifically state that these are the steps involved

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gentieu (US 6880070) in view of Hipp (US 20050111364)

Claim 1, 2, 7, 9 Gentieu discloses receiving at a first port **(fig1, 150, where a port by definition is merely a physical interface between a circuit and a device)** of the switch **(Col 1 line 24, communication device)** a packet that specifes a virtual target as a desintation.

Gentieu discloses sending at a second port **(fig 4, 440, where a port by definition is merely a physical interface between a circuit and a device)** of the switch the packet to a physical target that is associated with the virtual target.

Gentieu discloses wherein steps a and b occur without buffering and at wirespeed within the switch **(Col 2 lines 55-58 and Col 1 line 55)**.

Gentieu does not specifically disclose the data packet specifying a virtual target and switching the packet to a physical target that is associated with the virtual target.

It is understood in the art that network data contains a header which is comprised of source and destination information, where the destination information is equivalent to a virtual target, where the claim does not define the structure of virtual target or the information associated with it. Therefore any specified target may be considered a virtual target, and furthermore, a physical target is equivalent to a virtual target as no designated structure has been specified.

Hipp discloses the data packet specifying a virtual target **(para 0025, line 26, IP address)** and switching the packet to a physical target **(para 0025, line 28, allocating new port)** that is associated with the virtual target **(para 0026, line 4, mapping b/w ports).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the multiplexing means (fig 4, 150) with the processor as disclosed by Gentieu. The motivation for this combination is to support the communication between applications which use virtual ports.

Claim 2 Gentieu discloses wherein steps a and b further occur at wire speed **(Col 1 line 55).**

Claim 7 Gentieu does not specifically disclose wherein the packet is for a particular request, and wherein at least one trace tag is associated with the packet and identifies information associated with the request.

Hipp discloses wherein the packet is for a particular request, and wherein at least one trace tag is associated with the packet and identifies information associated with the request **(para 0031, since data is extracted at the second VPM and translated,**

the data being sent is equivalent to a request, and the AID or addresses are equivalent to a trace tag specifying information about the data).

Claims 3, 4, 5, 6, 8 10, 11, 12, 13, 34, 35, 24, 25, 26, 29 , 30, 31, 32, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gentieu (US 6880070) in view of Hipp (US 20050111364) in firther view of Morgan (US 5524254)

Claim 3, 8 Gentieu does not specifically disclose wherein the first port is located on a first linecard and wherein the second port is located on a second linecard, the first linecard forwarding the packet to the second linecard along with information about the virtual target, the second linecard utilizing the information about the virtual target to update the packet with an address of a physical target.

Hipp discloses a first port **(p1 in fig 6)** forwarding the packet to a second port **(para 0031, lines 10-14, first port forwards data to second VPM, where the second VPM is directly associated with the second port P2)** along with information about the virtual target **(para 0031 lines 19-21m desitnation address).**

Hipp discloses the second port (para 0031, line 13, the second VPM i is directly associated with the second port) utilizing the information about the virtual target to update the packet with an address of a physical target (para 0031 lines 13-14 and lines 19-21), where the translation involves translating form a first virtual port to a detaintion IP address and port).

The combined teachings of Gentieu and Hipp do not specifically disclose first and second ports being located on first and second linecards respectively.

Morgan discloses ports being located on a linecard as disclosed in **fig 5, element 74a and 74b.**

Regarding claim 8, Hipp discloses a plualrity of port and a multiplexing system, where it would have been obvious to one of the ordinary skill in the art that the combined teachings is applicable to a plurality of linecards in connection such as those shown in fig 5 of Morgan.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the combined teachings of Gentieu and Hipp, to provide the discussed components on a line card such as that shown in fig 5 of Morgan. The motivation for this modification is to support the physical and data link layer of communication, and support different services **(Col 3 lines 22-30).**

Claim 4 Gentieu does not specifically disclose wherein the information about the virtual target is obtained from a virtual target descriptor.

Hipp discloses wherein the information about the virtual target is obtained from a virtual target descriptor **(para 0031 lines 15-21, where the information being extracted and translated is obtained from the transmitted data, and describes the virtual destination).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the inventionof Gentieu so as to contain destination information as disclosed by Hipp. The motivation for this modification is to specify a destination for routing **(Hipp para 0023 lines 22-23).**

Claim 5, 6 Gentieu does not specifically disclose the information about the virtual target being obtained from a virtual target descriptor stored in a memory on the first linecard.

Hipp discloses the information about the virtual target being obtained from a virtual target descriptor stored in a memory on the first linecard **(fig 6 shows a first VPM and a second VPM being connected to a first port p1 and second port P2 respectively, and steps 12 and 13 in fig 6 show a table).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the processor as disclosed by Gentieu so as to implement VPM routing and adding a VPM to the ports as disclosed by Hipp. The motivation for this modification is to virtually route data from one device to another.

Claim 10, 11, 12, 13, 34, 35, 24-33 Gentieu discloses receiving at a first port **(fig1, 150, where a port by definition is merely a physical interface between a circuit and a device)** of the switch **(Col 1 line 24, communication device)** a packet that specifes a virtual target as a desintation.

Gentieu discloses sending at a second port **(fig 4, 440, where a port by definition is merely a physical interface between a circuit and a device)** of the switch the packet to a physical target that is associated with the virtual target.

Gentieu discloses wherein steps a and b occur without buffering and at wirespeed within the switch **(Col 2 lines 55-58 and Col 1 line 55)**.

Gentieu does not specifically disclose the data packet specifying a virtual target and switching the packet to a physical target that is associated with the virtual target.

It is understood in the art that network data contains a header which is comprised of source and destination information, where the destination information is equivalent to a virtual target, where the claim does not define the structure of virtual target or the information associated with it. Therefore any specified target may be considered a virtual target, and furthermore, a physical target is equivalent to a virtual target as no designated structure has been specified.

Hipp discloses the data packet specifying a virtual target **(para 0025, line 26, IP address)** and switching the packet to a physical target **(para 0025, line 28, allocating new port)** that is associated with the virtual target **(para 0026, line 4, mapping b/w ports).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the multiplexing means (fig 4, 150) with the processor as disclosed by Gentieu. The motivation for this combination is to support the communication between applications which use virtual ports.

Gentieu does not specifically disclose wherein the first port is located on a first linecard and wherein the second port is located on a second linecard, the first linecard forwarding the packet to the second linecard along with information about the virtual target, the second linecard utilizing the information about the virtual target to update the packet with an address of a physical target.

Hipp discloses a first port **(p1 in fig 6)** forwarding the packet to a second port **(para 0031, lines 10-14, first port forwards data to second VPM, where the second**

VPM is directly associated with the second port P2) along with information about the virtual target **(para 0031 lines 19-21m desitnation address).**

Hipp discloses the second port (para 0031, line 13, the second VPM i is directly associated with the second port) utilizing the information about the virtual target to update the packet with an address of a physical target (para 0031 lines 13-14 and lines 19-21), where the translation involves translating form a first virtual port to a detaintion IP address and port).

The combined teachings of Gentieu and Hipp do not specifically disclose first and second ports being located on first and second linecards respectively.

Morgan discloses ports being located on a linecard as disclosed in **fig 5, element 74a and 74b.**

Regarding claim 8, Hipp discloses a plualrity of port and a multiplexing system, where it would have been obvious to one of the ordinary skill in the art that the combined teachings is applicable to a plurality of linecards in connection such as those shown in fig 5 of Morgan.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the combined teachings of Gentieu and Hipp, to provide the discussed components on a line card such as that shown in fig 5 of Morgan. The motivation for this modification is to support the physical and data link layer of communication, and support different services **(Col 3 lines 22-30).**

Claim 27 Gentieu discloses the processor unit including a packet aggregation and classififcation engine **(fig 1, 120, as no given function or structure has been given**

to the claimed unit) and a packet processor unit **(fig 1, 110, as no given function or structure has been given to the claimed unit).**

Claim 28 Gentieu discloses instruction memory, where an SRAM or CAM may be used depending on a designers preference/choice **(fig 1, 160).**

3. Claims 14, 15, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tzeng (US 6693906) in view of Latif et al. (US 640030), hereinafter referred to as Latif.

Claim 14 Tzeng discloses receiving a packet at an ingress port (element 20 in fig 1), the packet being destined for a virtual target with a virtual target address

Tzeng discloses forwarding the packet to a fabric (element 25 in fig 1), which forwards the packet to an egress port in accordance with address information (see fig 1 and description)

Tzeng discloses sending a packet at an egress port (any of elements 20 in fig 1).

Tzeng discloses sending at a second port the packet to a physical target that is associated with the virtual target (Col 3 lines 33-59 and see fig 1 including all of the shown ports), where the VLAN information and Layer 3 switching is used to route data to a destination.

Tzeng does not specifically disclose each port associated with a line card, information including a flowID, and placing a virtual target descriptor identifier and the flow ID in a local header (fig 6a and 6c port ID);

Latif discloses each port associated with a line card (see figs 5, 6a, 6c, Col 7 line 47-Col 8 line 61), information including a flowID, and placing a virtual target descriptor identifier and the flow ID in a local header (fig 6a and 6c port ID).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the ports as disclosed by Tzeng to be applied with the line cards as disclosed by Latif. The motivation for this modification is to allow the switch the intelligence to determine the type of traffic and direct it accordingly (Col 19 lines 25-30).

Claim 15 Tzeng discloses the packet being for a particular request, and wherein at least one trace tag is associated with the packet and identifies information associated with the request (Col 5 lines 18-58).

Claim 17 Tzeng discloses the steps of receiving and sending as described above occurring without buffering the packet (Col 1 lines 39-Col 2 line 6 and Col 5 lines 35-51 and Col 8 lines 52-67).

Claim 18 Tzeng does not specifically disclose the virtual target descriptor being stored in an SRAM on the ingress line card and the virtual target descriptor identifier being stored in a CAM on the ingress line card.

Latif discloses a direct memory access block within fig 20.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the ports as disclosed by Tzeng to be applied with the line cards as disclosed by Latif. The motivation for this modification is to allow the switch the intelligence to determine the type of traffic and direct it accordingly (Col 19 lines 25-30).

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tzeng (US 6693906) in view of Latif et al. (US 640030), hereinafter referred to as Latif in further view of Gentieu (US 6880070).

Claim 16 The combined teachings of Tzeng and Latif do not specifically disclose wherein all of the steps are performed at wire speed.

Gentieu discloses a processor performing functions at wire speed **(Col 1 line 55, where the preceding claims do not specify which steps are associated with the wire speed as indicated by the 112 rejection).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine wire speed transmission in any device for fast communication.

Allowable Subject Matter

5. Claims 19-23 are allowed.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P. Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 10AM-7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on (571)272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher Grey
Examiner
Art Unit 2616

4/24/07

DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600